In the Claims:

1. (Currently Amended) A method for forming a dual damascene metal interconnection of a semiconductor device, comprising:

forming an interlayer insulation layer and a polishing buffer layer on a semiconductor substrate; then

etching the interlayer insulation layer and the polishing buffer layer to form a via hole; then

forming a sacrificial filling film on the polishing buffer layer to fill the via hole; then

etching the sacrificial filling film, the polishing buffer layer and the interlayer insulation layer to form a trench, thereby forming a dual damascene pattern including the via hole and the trench; then

forming an etching buffer layer on a sidewall of the trench; then

removing at least some of the sacrificial filling film in the via hole; and then

forming a metal interconnection within the dual damascene pattern.

2. (Original) The method according to Claim 1, wherein the sacrificial filling film comprises a flowable oxide.

3. (Original) The method according to Claim 1, wherein the etching buffer layer acts as a protective film for protecting the interlayer insulation layer while removing at least some of the sacrificial filling film in the via hole.

4. (Original) The method according to Claim 1, wherein the etching buffer layer is comprised of a material having an etching selectivity to the sacrificial filling film.

5. (Original) The method according to Claim 4, wherein the etching buffer layer comprises a barrier metal film such as TiN and Ta.

6. (Original) The method according to Claim 4, the etching buffer layer comprises an insulation film such as a nitride film.

7. (Original) The method according to Claim 1, wherein the metal interconnection forming step comprises:

removing the etching buffer layer;

depositing a barrier metal film and a metal film to fill the dual damascene pattern; and

etching the barrier metal film and the metal film through a chemical mechanical polishing process using the polishing buffer layer to form the metal interconnection including the barrier metal film.

8. (Original) The method according to Claim 1, wherein the metal interconnection forming step comprises:

depositing a barrier metal film and a metal film to fill the dual damascene pattern including the etching buffer layer; and

etching the barrier metal film and the metal film through a chemical mechanical polishing process using the polishing buffer layer to form the metal interconnection including a dual barrier metal film.

9. (Original) The method according to Claim 8, wherein the metal interconnection includes the dual barrier metal film which includes the etching buffer layer comprised of a barrier metal film and the barrier metal film, and the metal film.

10. (Currently Amended) A method for forming a dual damascene metal interconnection of a semiconductor device, comprising:

forming sequentially a first etch stop layer, a first interlayer insulation layer, a second etch stop layer, a second interlayer insulation layer, and a polishing buffer layer on a semiconductor substrate; then

etching the first and second interlayer insulation layers, the second etch stop layer and the polishing buffer layer to form a via hole; then

forming a sacrificial filling film on the polishing buffer layer to fill the via hole; then

etching the sacrificial filling film, the polishing buffer layer, the second interlayer insulation layer and the second etch stop layer to form a trench, thereby forming a dual damascene pattern including the via hole and the trench; then

forming an etching buffer layer on a sidewall of the trench; then

removing a remaining sacrificial filling film in the via hole; then

removing the first etch stop layer within the via hole; and then

forming a metal interconnection within the dual damascene pattern.

11. (Original) The method according to Claim 10, wherein the etching buffer layer acts as a protective film for protecting the second interlayer insulation film while removing the sacrificial filling film in the via hole.

12. (Original) The method according to Claim 10, wherein the etching buffer layer is comprised of a material having an etching selectivity to the sacrificial filling film.

13. (Original) The method according to Claim 12, wherein the etching buffer layer comprises a barrier metal film such as TiN and Ta.

14. (Original) The method according to Claim 12, wherein the etching buffer layer comprises an insulating film such as a nitride film.

15. (Original) The method according to Claim 10, wherein the metal interconnection includes:

a first barrier metal film for the etching buffer layer formed on the sidewall of the trench;

a second barrier metal film formed within the dual damascene pattern; and

a metal film filled within the dual damascene pattern.

16. (Original) The method according to Claim 10, wherein the metal interconnection includes:

a barrier metal film formed within the dual damascene pattern; and

a metal film filled within the dual damascene pattern.

17. (Original) The method according to Claim 10, further comprising removing the etching buffer layer, after removing the first etch stop layer.

18. (Withdrawn) A dual damascene metal interconnection of a semiconductor device, comprising:

a semiconductor substrate;

an interlayer insulation layer including a dual damascene pattern a comprising via hole and a trench on the semiconductor substrate;

a first barrier metal film on a sidewall of the trench;

a second barrier metal film within the dual damascene pattern; and

a metal film that fills the dual damascene pattern.

19. (Currently Amended) A method of forming a metal interconnection for an integrated circuit device, comprising:

forming a trench in an integrated circuit substrate and a via hole beneath a portion of the trench, the trench including a trench sidewall and the via hole including a sacrificial film therein; then

forming a buffer layer on the trench sidewall; then

removing at least some of the sacrificial film from the via hole by etching the sacrificial film through the trench that includes the buffer layer on the trench sidewall; and then

forming the metal interconnection in the via hole from which at least some of the sacrificial film has been removed, and in the trench.

20. (Original) A method according to Claim 19 wherein the buffer layer comprises material having etch selectivity to an etchant which is used in the removing, to thereby protect the trench sidewall during the removing.

21. (Original) A method according to Claim 19 wherein the buffer layer comprises a conductive buffer layer.

22. (Original) A method according to Claim 19 wherein the following is performed between the removing and the forming the metal interconnection:

removing the buffer layer from the trench sidewall.

23. (Original) A method according to Claim 19 wherein the forming a buffer layer comprises:

forming a buffer layer on the trench sidewall that does not extend into the via hole.

24. (Withdrawn) An integrated circuit comprising:

an integrated circuit substrate including a trench therein and a via hole beneath a portion of the trench, the trench including a trench sidewall;

a sacrificial film in the via hole; and

a buffer layer on the trench sidewall.

25. (Withdrawn) An integrated circuit according to Claim 24 wherein the buffer layer comprises material having etch selectivity to an etchant of the sacrificial film.

26. (Withdrawn) An integrated circuit according to Claim 24 wherein the buffer layer comprises a conductive buffer layer.

27. (Withdrawn) An integrated circuit comprising:

an integrated circuit substrate including a trench therein and a via hole beneath a portion of the trench, the trench including a trench sidewall;

a conductive buffer layer on the trench sidewall that does not extend into the via hole; and

a metal interconnection in the via hole and in the trench.

28. (Withdrawn) An integrated circuit according to Claim 27 wherein the metal interconnection comprises:

a first metal film that extends conformally on the conductive buffer layer and in the via hole; and

a second metal film on the first metal film that fills the trench and the via hole.